DESIGN OF MAGNETIC DRUM MEMORY SYSTEM

BY

MAJOR N. C. DATTA

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR
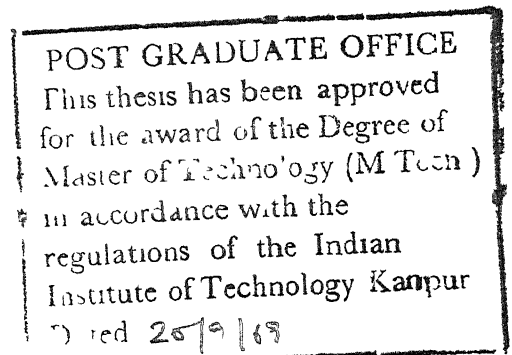
AUGUST, 1969

DESIGN OF A MAGNETIC DRUM MEMORY SYSTEM

A Thesis submitted

in partial fulfilment of the requirements

for the degree of

Master of Technology

by

Major N. C. DATTA

to the

Department of Electrical Engineering

Indian Institute of Technology

Kanpur

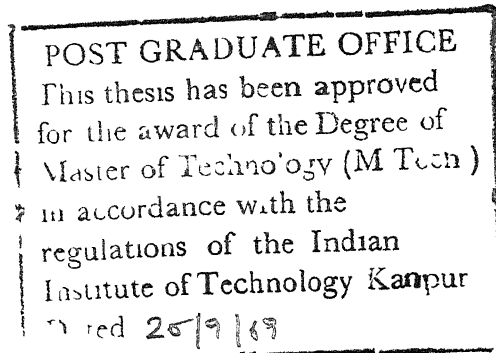August 1969

DESIGN OF A MAGNETIC DRUM MEMORY SYSTEM

A Thesis submitted

in partial fulfilment of the requirements

for the degree of

Master of Technology

by

Major N. C. DATTA

to the

Department of Electrical Engineering

Indian Institute of Technology

Kanpur

August 1969

This is to certify that this work on DESIGN OF A MAGNETIC DRUM MEMORY SYSTEM has been carried out under my supervision and it has not been submitted elsewhere for a degree.

/

R. N. Biswas
Department of Electrical Engineering
Indian Institute of Technology
Kanpur

ACKNOWLEDGEMENT

I am grateful to Dr. R. N. Biswas for his constant help and guidance during the Project work.

I would also like to take this opportunity to thank Dr. T. R. Viswanathan and Dr. V. Rajaraman for making valuable suggestions.
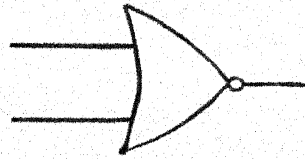
ABSTRACT

For high speed computers it is always desirable to provide a large capacity buffer memory to backup the high speed working memory.

This thesis concerns with the design of a flexible magnetic drum memory system able to handle upto a maximum of 3912 bits and 1023 words per track at a bit repitition rate which can have a maximum value of 1 MHz. The complete logic circuits have been built by making use of Motorola Integrated Circuits and discrete components have been used in making Read/Write amplifiers and the gates.

TABLE OF CONTENTS
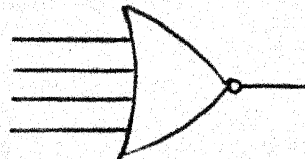
LOGIC SYMBOLS

TWO INPUT NOR

FOUR INPUT NOR

INVERTING AMPLIFIER

NON-INVERTING AMPLIFIER

CLEAR DIRECT

PULSE SET

TRIGGER

PULSE RESET

S
T
R

CD

0   1

FLIP-FLOP

Y

Ȳ
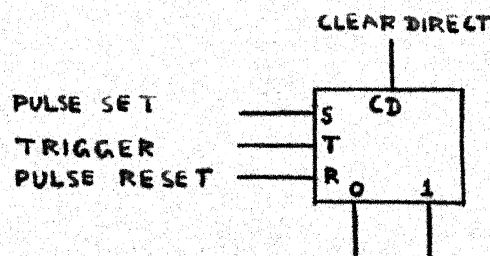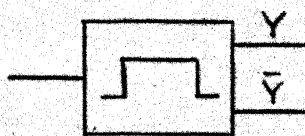
ONE SHOT MULTIVIBRATOR
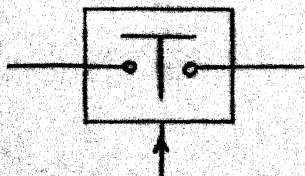
SIX DIODE GATE
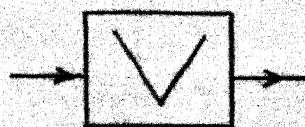
READ/WRITE AMPLIFIER

CHAPTER I

INTRODUCTION

Magnetic recording as a method of providing the function of memory has attained a major position in the field of digital data storage. Its most extensive applications are in the form of magnetic drum, magnetic-tape and magnetic-disk memory units.

Reasons for wide exploitation of magnetic recording are based upon its flexibility of mechanical structure, economy in terms of cost per-bit, compectness for large capacities and ruggedness.

Although it is only in recent years that magnetic recording has come into general use, its invention by the Danish engineer Valdemar Poulsen dates back to 1898. The first apparatus used a steel wire for the recording medium, while today, a thin magnetic layer is used exclusively for this purpose in the computer field. The actual work which marked the beginning of the application of magnetic recording to data storage was undertaken in 1947. The first practical unit was magnetic drum.

The various types of units in which magnetic recording provides the data storage differ between themselves

essentially only in the mechanical structure used to provide
relative motion between the surface and from one to many
electro-magnetic transducers.

A rotating drum whose surface possesses a magnetic-
recording film serves the function of a high-speed memory
for intermediate-size computers. Magnetic heads, located
slightly out of contact with the surface, allow information
to be read into and out of the drum. Drum speeds are in
the range of thousands of rpm, and in an average-sized drum
hundreds of thousands of binary digits can be stored with
an access time to any bit in the order of milliseconds.

Important aspects of magnetic recording with
respect to its use for data storage are the following:
saturation recording is used and, therefore, new information
may be written over that previously contained, erasing being
unnecessary; the memory is non-volatile, i.e., the information
is not lost in the event of a power failure; there is no
apparent deterioration of the recorded information with time;
and the storage film can tolerate considerable physical abuse
with no deleterious effects and is insensitive to wide
variations in environmental conditions.

1.1 Drum Storage Characteristics

A moving storage surface for binary information
can be specified in terms of its capacity in binary digits
(bits) and an inherent access time, which is taken here to

be the recurrence interval for a given bit of information.
For a rotating drum this interval is the time for one
revolution. The merit of the storage surface may be
measured by the ratio of capacity to access time as it is
advantageous to increase the capacity, decrease the access
time or both

$$\frac{C}{A} = \frac{v}{S} = p$$

where, C : capacity of track, bits.

A : inherent access time.

v : cell length or distance assigned to one bit
on the magnetic surface in the direction of
its rotation

S : linear speed of the drum surface.

p . information transfer rate, bits per unit time.

This ratio is then equal to the rate of information transfer
which is an external measure of memory quality.

1.2 Coding Techniques for Binary Storage

Binary storage coding techniques can be grouped
broadly into two categories. One group comprises those
methods which result in a useful output signal for every
bit, while the second includes those codes which provide a
useful output signal only upon a change in binary sequence
or, equivalently, only for one of the two binary digits.

The first group of codes is in a sense redundent in that the original binary sequence can be re-constructed, knowing only the first digit in addition to the changes in binary digit sequence. For any particular input current code the resulting output signal depends upon the recording system design and cannot be anticipated independently of this information. The choice of a particular code depends upon overall reliability and digital processing requirements.

The following diagram indicates schematically the overall storage transfer process involved in the magnetic recording of binary information. The peripheral co-ordinate is x

$$\underbrace{i(t) \dashrightarrow M(x)}_{\text{writing}} \underbrace{\longrightarrow}_{\text{reading}} sN\frac{d\varnothing_h}{dx} = e_o(t)$$

where $M(x)$: distribution of magnetization on the surface.

$\varnothing_h(x)$: reading coil flux as a function of the angular position of the drum.

s : surface speed.

e_o : open-circuit read-back output voltage.

N : number of reading turns.

The input current is associated with the recorded pattern through the airgap fringing field of the magnetic recording head. The output voltage can be directly related to a variation of core flux with drum angular position.

CHAPTER II

RECORDING TECHNIQUES

Recording techniques broadly refer to the methods
of writing and reading binary data. Writing involves the
translation of a binary sequence into a unique magnetising
current pattern and reading involves the detection of the
magnetisation present on the drum and its conversion into
the corresponding binary information. Data-recording
techniques can be divided into two categories, external
clocking and self-clocking. External clocking implies that
a clock track is provided to furnish all location and
writing is synchronized by these timing pulses. Self-
clocking recording methods, on the otherhand, are those in
which clocking information is derived from the recorded data,
no external clock track being used.

There are a number of ways to record binary
information on a magnetic surface. The various recording
techniques have their own advantages and disadvantages with
regard to: the circuit required, sensitivity to sources of
noise, reliability and density consideration. The different
methods used fall broadly into two classes: return to zero
and non-return to zero. In the former, the flux in the
surface always returns to a reference value between bits of

information; in the latter, the flux does not return to
reference value between digits. Since only two values of
information are being recorded (0 and 1), it is customary
to saturate the magnetic surface.

2.1 R Z Recording

True return to zero recording (Fig. 2.1) uses a
round-trip excursion from zero flux to one saturation level
to represent binary 0 and a round-trip excursion to the
other saturation level to represent binary 1. The flux
departs from the zero flux state and goes to saturation
and returns for each digit recorded. We see that there
are two pulses in the read-back signal corresponding to the
two flux changes for each binary digit recorded - zero to
saturation and saturation back to zero. In this scheme,
therefore, there is more information present then is
really needed.

2.2 N R Z Recording

R Z recording identifies a digit with a flux
excursion from a reference state to a saturation state and
back. Non-returns-to zero (N R Z) recording (Fig.2.2)
identifies a digit with a flux level, rather than with a
change of flux. If flux at one saturation level represents
0, flux at the opposite saturation level then represents 1.

If a string of digits of like kind is being recorded, the
flux remains unchanged at the saturation level even between
the digits. The flux changes only when successive digits
are unlike. The read-back signal thus consists of pulses
which have one polarity for a '0' following a '1' and the
other polarity for the reverse sequence. We see that the
maximum number of flux changes occurs when the digit pattern
alternates 0's and 1's, and that even under this condition,
the number of changes of flux is half what it would be in
a R Z system. N R Z recording is, therefore, capable of
at least twice the packing density of an R Z system.

2.3 N R Z I Recording

This is a form of recording which belongs to the
generic class of N R Z type techniques; the I stands for
inversion. It records one of the two binary digits(say '1')
as a single flux change, while the other (i.e., '0') has no
corresponding flux change. Hence the same digit ('1') is
sometimes indicated by a positive signal from the head, and
sometimes by a negative signal. As with the previous N R Z
scheme, the maximum number of changes of flux is half what
it would have been in R Z.

2.4 Phase Recording

Phase recording (Fig.2.4) is again an N R Z type
system, in that the flux is always in one of the saturation
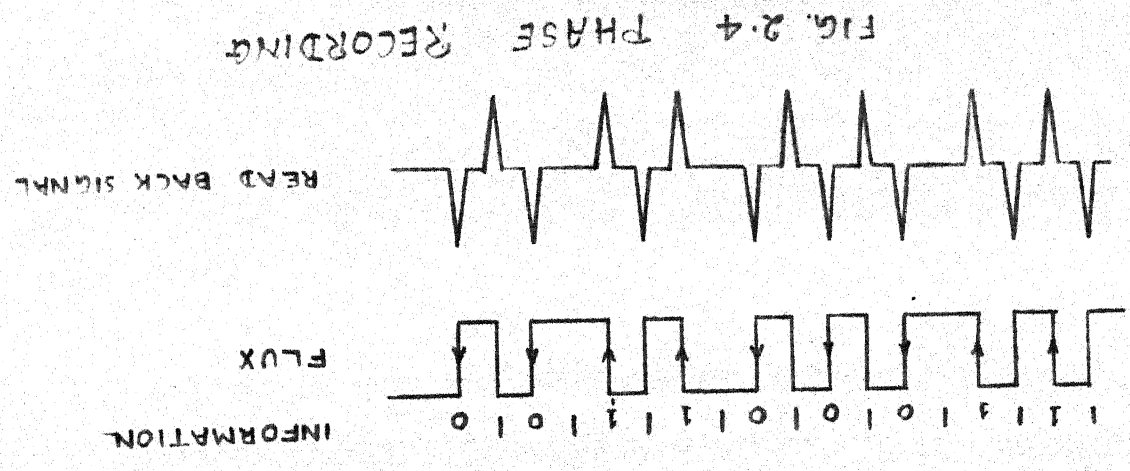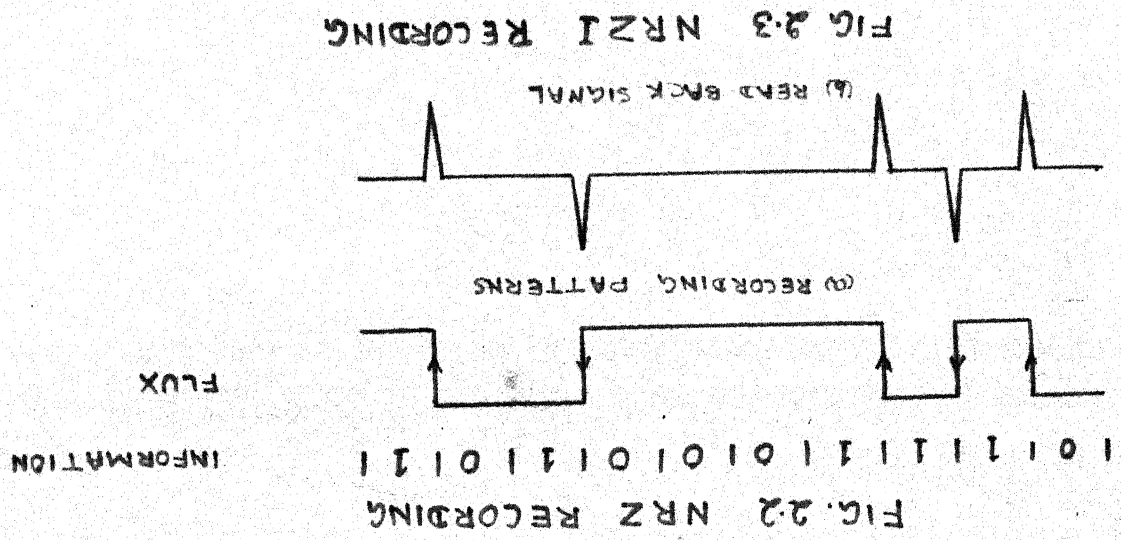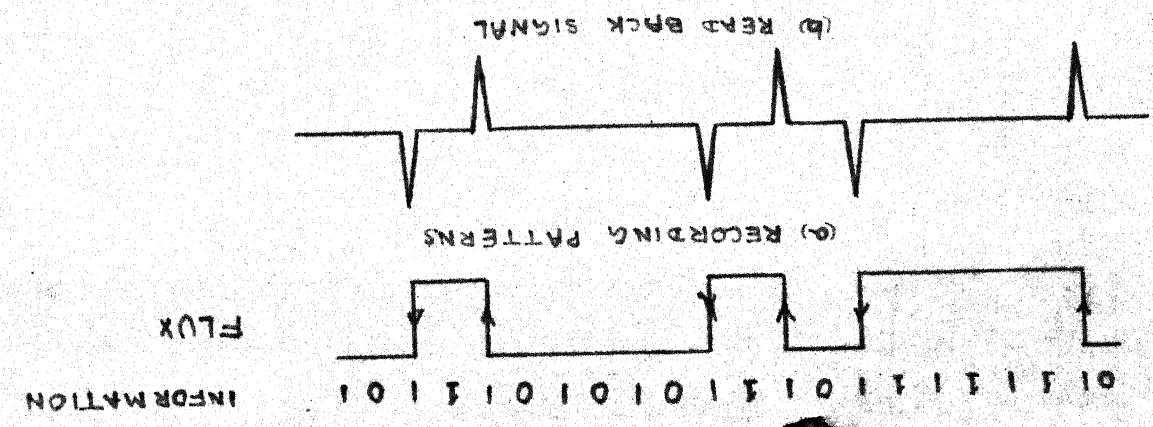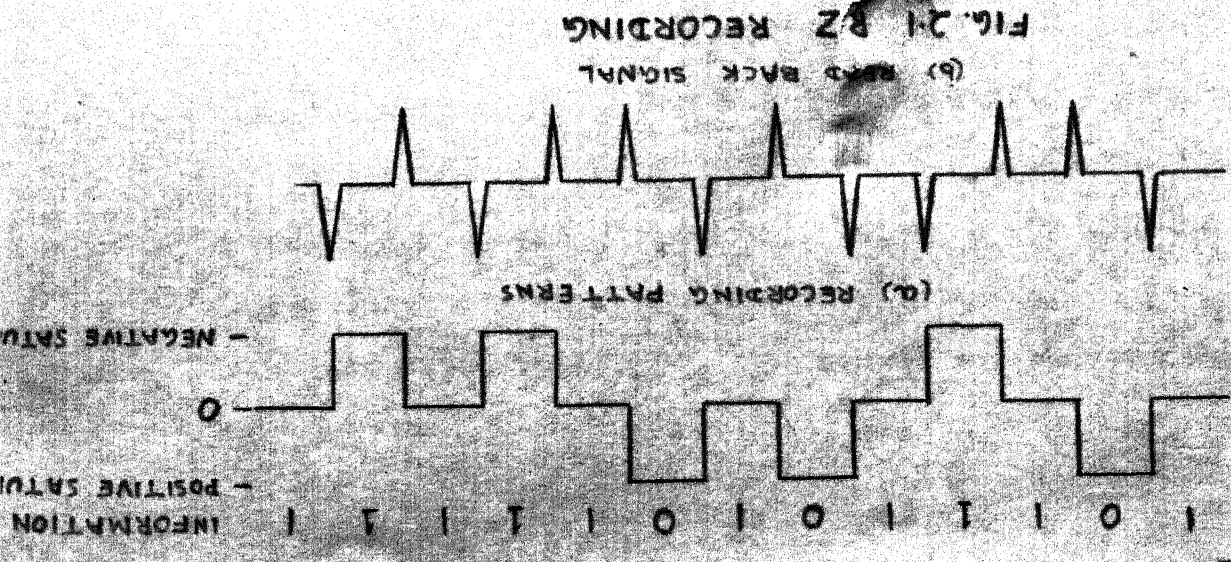
states except during the transition, but its difference
from the ordinary N R Z scheme lies in the fact that the
digits correspond to transitions in the flux levels rather
than to the levels themselves. The two binary digits are
represented by opposite changes in the flux level from one
saturation level to the other. In the pattern shown in
Fig.2.4, a '1' has been represented by a transition from
the higher saturation level to the lower (the names 'higher'
and 'lower' being, ofcourse, quite arbitrary), the
representation of a '0' then being the reverse transition.
The important point is that the transitions take place at
the centres of the digit intervals.

Each bit of information is thus represented by a
pulse in the read-back signal, the polarity of the pulse
being different for the two digits. However, in addition
to these pulses representing the information, the read-
back signal also contains a pulse at each junction of two
like digits. Any reading scheme for phase recording
technique, therefore, has to eliminate these unwanted
pulses before the stored information can be recovered. It
is clear that the lowest frequency of the flux pattern
occurs for an alternating digit pattern and the highest
frequency, for an unchanging digit pattern. One of these
is twice the frequency of the other, and therefore the

maximum and minimum frequency components which can occur in
a system of this kind are readily determined. Furthermore,
there is no D-C component in the write current. In the
usual N R Z scheme there can be substential low frequency
components. For example, suppose the reference digit is 1,
for a sequence of words, each containing all 1's, the current
in the head stays quiescent at the 1 level.

CHAPTER III

OVERALL SYSTEM DESIGN

3.1 The Layout

The block diagram of Fig.3.1 shows the general
arrangements of the major functional blocks essential for
the operation of a typical serial access magnetic drum
memory.

The inputs to the decoder and to the coincidence
unit are obtained from the Memory Address Register. This
register stores the address of the location where information
is to be retrieved from or inserted in. The address of a
word on a drum is in two parts, a number specifying the
track and a number specifying the sector of the track in
which the required word is located. A drum is a sequential
access system in which time acts as one of the selection
co-ordinates. It is therefore, necessary to keep an
accurate count of words as they pass the magnetic head so
that any word can be located. Each sector, which corresponds
to one storage location on a track, is marked by a pulse
recorded on a separate word-clock track. These pulses are
then sensed in a counter until the counter registers the
number of words in each track. After this predetermined
maximum count the counter is automatically reset to 0, so
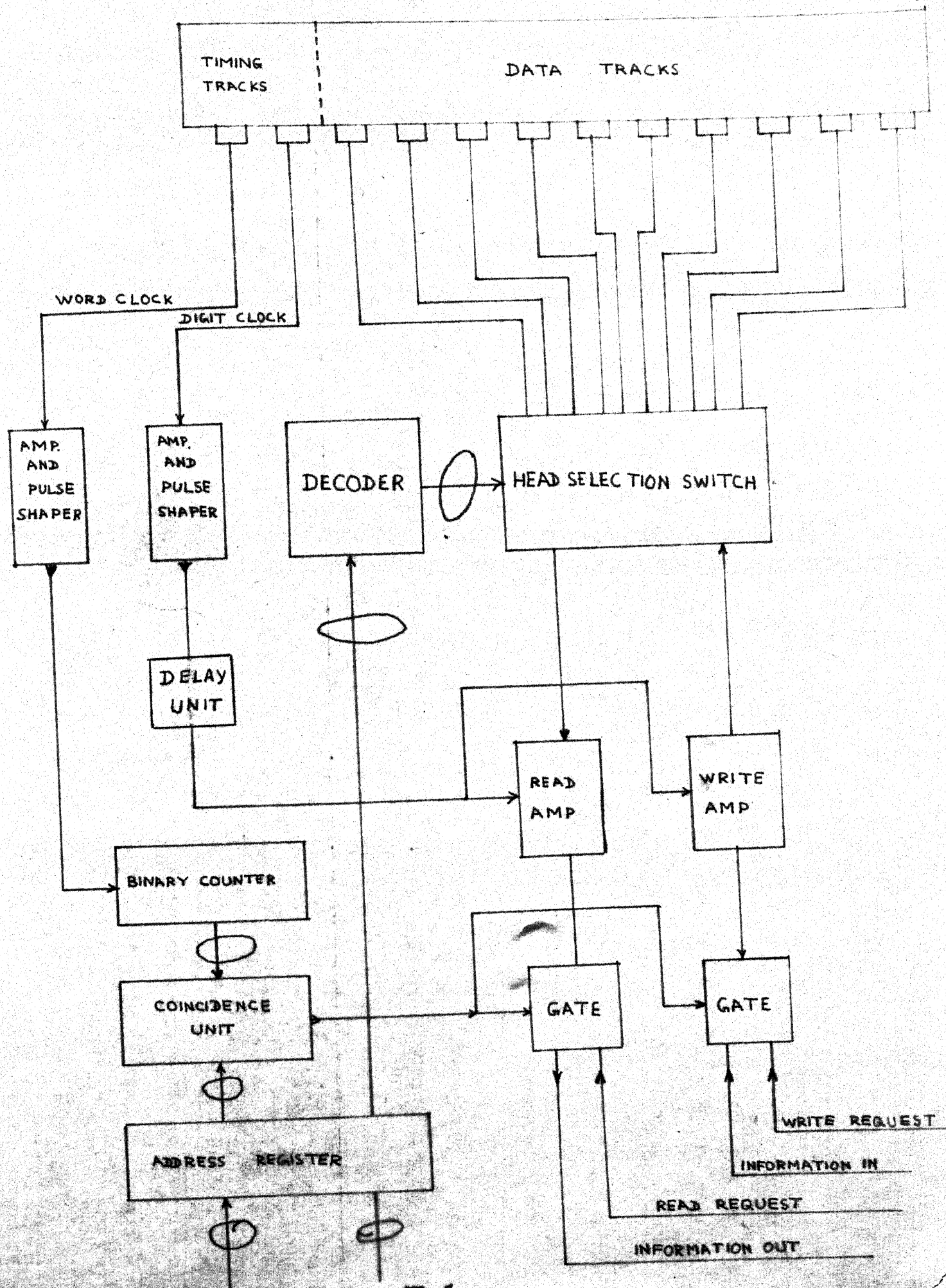
FIG 3·1

that any sector of the drum is uniquely determined by the
number recorded by the counter. When coincidence occurs
between the counter reading and the address of the required
sector as registered in the Address Register either the
read gate is opened, allowing the required word of
information to pass from the store, or the write gate is
opened, allowing new information to be written on the
proper sector of the drum surface. The remaining digits
in the Address Register specify the track number and, when
decoded they control the head selection switch.

To synchronize the strobe signal required for
reading and writing with the drum rotation rate, a separate
track is used to record the clock pulses permanently. For
reasons which will be explained later, these clock pulses
have been delayed by half the interval between adjacent
clock pulses, before they are used in Read and Write
amplifiers.

3.2 Specification of the Drum Unit

Number of available heads = 14.

Head specifications:

Number of turns = 150

Inductance at 140 KHz = 310 uh $\pm$ 15%

Self-resonant frequency = 1.6 MHz

Maximum direct current rating = 250 ma

14

MILLI VOLTS PER TURN PER THOUSAND INCHES PER SECOND

.6
.5
.2
.1
.06
.04
.02

50 80 100   200 300

PULSES PER INCH
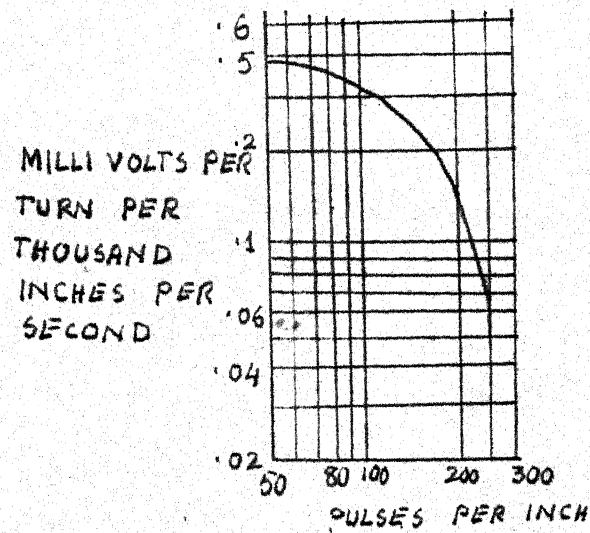
FIG 3.2 PLAYBACK VS PULSE DENSITY.

MILLIVOLTS PER TURN PER THOUSAND INCHES PER SECOND

.4
.2
.1
.08
.06
.04
.02
.01

50 PPI
100 PPI
125 PPI
150 PPI
200 PPI
250 PPI

40 60 80 100 150 200

WRITE CURRENT ma O.P.
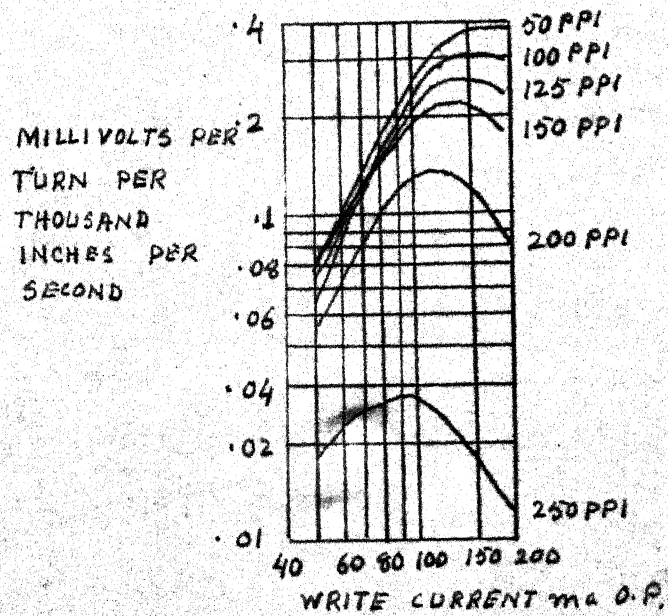
FIG 3.3 PLAYBACK VS CURRENT.

Drum specifications:

(a) Diameter = 5"

(b) Speed of rotation = 3600 rpm

(Surface speed = 942"/sec.)

(c) The relationship between play-back voltage

vs.pulse density is shown in Fig.3.2.

(d) The relation between the play-back voltage

vs. head current is shown in Fig.3.3.

3.3 General Design Considerations

Our aim here is to keep the design as flexible as possible so as to obtain a versatile general-purpose memory system. The general procedure for setting up the drum memory for any particular application is as follows.

(a) Clock pulses at the desired bit repetition

rate are first recorded in the (digit)clock

track.

(b) Word-clock pulses, obtained by properly scaling

the frequency of the clock pulses according to

the word length, are next recorded in the word-

clock track.

(c) A suitable pulse density (P P I) is chosen to

give the desired compromise among write current,

play-back voltage and pulse density as shown by

Figs. 3.2. and 3.3.

(d) The write amplifier is adjusted to give the
optimum write current (Fig.3.3) for maximum
play-back voltage for the chosen pulse density.

(e) The delay unit is adjusted to delay the clock
pulses by approximately half the interval
between adjacent clock pulses.

(f) Adjustments are made to ensure that any of the
gates, once opened, remains so for the duration
of a word.

(g) The word counter is adjusted so that its
contents are automatically cleared upon
reaching a count equal to the number of words
per track.

As seen easily from the play-back voltage speci-
fications given in the preceding section (Figs. 3.2 and 3.3),
the maximum permissible pulse density is 250 P P I. Combining
this with the surface speed of the drum, we obtain the
maximum pulse repetition rate = 942 x 250 = 235.5 KHz. This
corresponds to a time-period of 4.26 μsec. In phase recording,
as indicated in Fig.2.4, there can at most be one pulse of
magnetisation per digit. Hence for our scheme of reading,
minimum bit width = 4.26 usec. This makes the maximum number
of bits per track equal to   3912.

One is seldom interested in word-lengths smaller
than 4 bits, so that, if one allows one bit between words, the

maximum number of words per track becomes $\frac{3912}{5} = 782$.

Thus in order to allow the word-length to be adjustable, we have to design the word-counter, the address-register as well as the coincidence unit on the basis of 10 bits. The system as such is thus capable of handling up to a maximum of 1023 words per track.

As an example, if we require a system with 8 bit word length and a bit repetition rate of 200 KHz., the counter has to be arranged to count 368. (Since the number of pulses per inch of the drum is 212, the total number of pulses on each track is 3320. Hence the number of 8-bit-words per track will be 368). From Fig.3.3 we see that at this bit repetition rate the write current required is of 120 illiamps. The delay in the clock pulses has to be 2.5 usec and the duration of all the gates have to be of 42 usecs.

Since 10 tracks have been used for Writing/Reading information, 4 flip-flops are required for addressing any one of the ten tracks. Consequently the Address Register consists of 14 flip-flops - 10 flip-flops for specifying the sector number and four for the track number. This completes the detailed requirements for a maximum of 1023 words per track of the memory.

3.4 Read-Write Scheme

Phase recording techniques has been choosen for
recording the binary information on the magnetic drum surface.
The desired flux pattern is achieved by using the delayed
clock pulse (delayed by half the interval between adjacent
pulses). Suppose it is desired to write 1110001100101O, the
corresponding pattern in phase recording will be as shown in
Fig.3.4. From the pattern it can be observed that writing
a '1' after a '0' or a '0' after a '1' can easily be done by
switching a flip-flop by the incoming information pulses. For
writing a string of consecutive '1's or a string of
consecutive '0's it is essential to sense the information well
in advance so that the output of the write amplifier is at the
negative saturation level in case the next information is a
'0' or at the positive saturation level in case the next
information is a '1'. The delayed clock-pulses can
conveniently be used to switch the write amplifier to the
desired saturation level before the arrival of the next bit
of information.

As the signal comes from the drum, it is of the
order of small fractions of a volt; it likely contains noise
and it is poorly shaped. The signal from the head is first
amplified and then shaped. The resulting signal is then
strobed at the centre of each digit interval; a positive
signal indicates a '0'; a negative signal, a '1'.

14
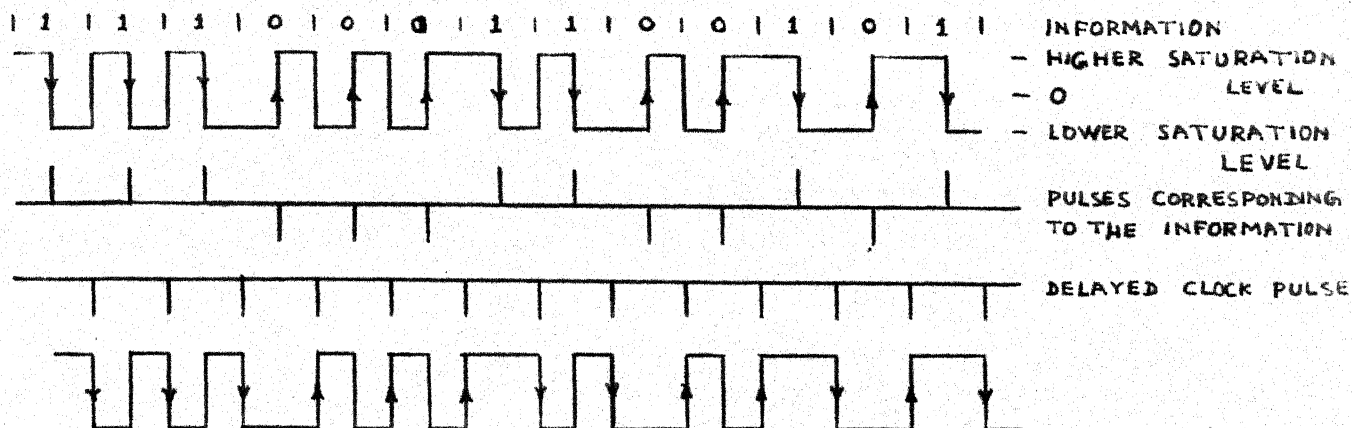
FIG 3.4 (a) PATTERN IN PHASE RECORDING
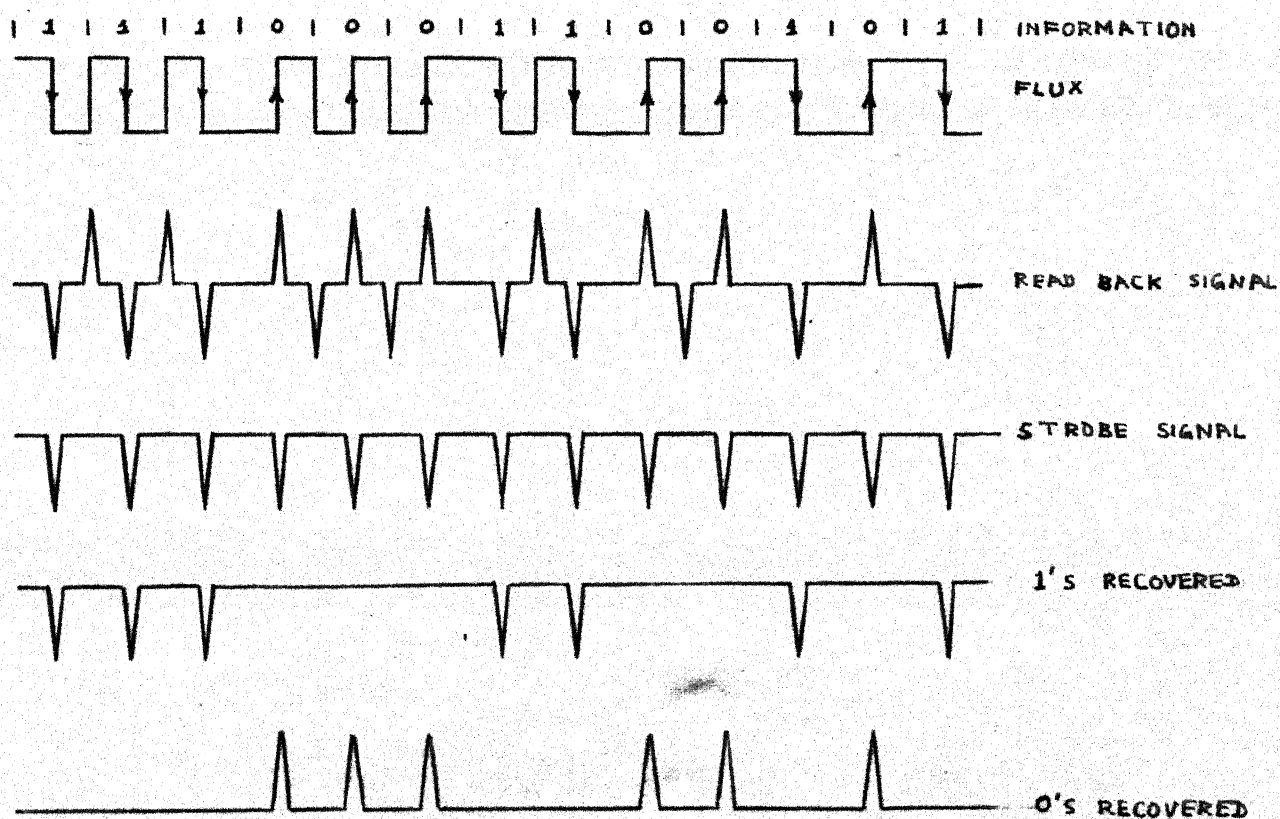
FIG. 3.4 (b)

INFORMATION RECOVERY FROM THE PHASE-RECORDED
READ BACK SIGNAL

CHAPTER IV

MEMORY PERIPHERAL CIRCUITS

The reliability of the complete system depends upon the efficient design of the peripheral circuits. These circuits are discussed in some detail in this chapter.

4.1 The M A R

The memory address register is required to hold the information temporarily during processing. Basically it consists a set of flip-flops either connected in series to form a serial bit register, or all the input lines have been kept independent to form a parallel bit register. Information is entered into or retrieved from such a register a word at a time.

M A R, in the present design, is of fourteen bit parallel register. The flip-flops used are of Motorola dual J K flip-flop (MC 890-P).

4.2 Coincidence Unit

To recognize that the address on the drum matches the address in the Address Register, the machine needs an equality comparison circuit, i.e , the comparison circuit for each pair of bits should have an output '1' when the

two bits being compared are either both '0' or both '1'.
This output is clearly the complement of the output of a
half-adder having the same bits as the two inputs, as seen
from the following truth table.

	A	0	0	1	1
	B	0	1	0	1
Coincidence output	C	1	0	0	1
Half-adder output	S	0	1	1	0

The Boolean expression for the above is given by

$$C = A\,B + \overline{A}\,\overline{B} = \overline{A\,\overline{B} + \overline{A}\,B} = \overline{S}$$

which can, therefore, be realised by using three N O R gates
as shown in Fig.4.1. One of these circuits is required for
each pair of digits which must be read together and for a
group of ten binary digits ten such comparators are needed.

The outputs from all the coincidence units are fed
to a ten-input AND gate to get a coincidence signal. This
coincidence signal is used to trigger a monostable
Multivibrator which inturn opens the input/output gates.
In Fig.4.2 S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8, S_9, S_{10} are the
inverted output from the ten coincidence unit. One dual
four-input NOR gate (MC 825-P) and one quad two-input
NOR gate have been used to make the ten-input AND gate.

$A\bar{B}$

$\overline{A\bar{B}+\bar{A}B}=\bar{S}$

$S = A\bar{B}+\bar{A}B$

$\bar{A}B$

FIG 4·1 HALF ADDER

S_1
S_2
S_3
S_4

$\bar{S_1}\bar{S_2}\bar{S_3}\bar{S_4}$

$\bar{S_1}\bar{S_2}\bar{S_3}\bar{S_4}\bar{S_5}\bar{S_6}\bar{S_7}\bar{S_8}$

S_5
S_6
S_7
S_8

$\bar{S_5}\bar{S_6}\bar{S_7}\bar{S_8}$

$\bar{S_1}\bar{S_2}\bar{S_3}\bar{S_4}\bar{S_5}\bar{S_6}\bar{S_7}\bar{S_8}\bar{S_9}\bar{S_{10}}$
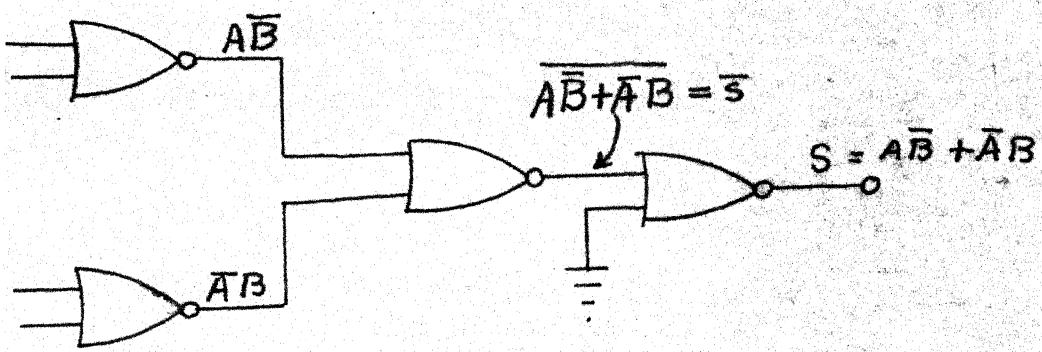
S_9
S_{10}
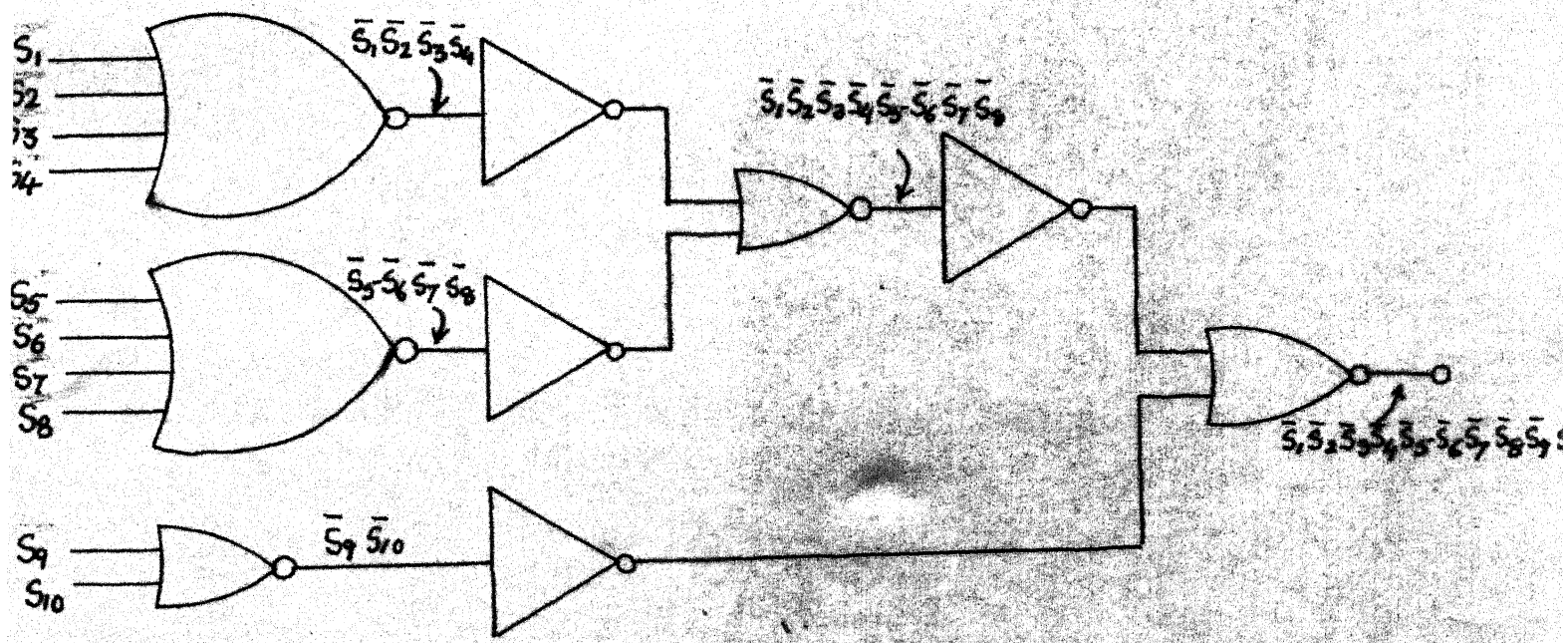
$\bar{S_9}\bar{S_{10}}$

FIG 4·2 TEN INPUT AND GATE

FIG. 4.3 COUNT OF 500

WORD PULSE INPUT
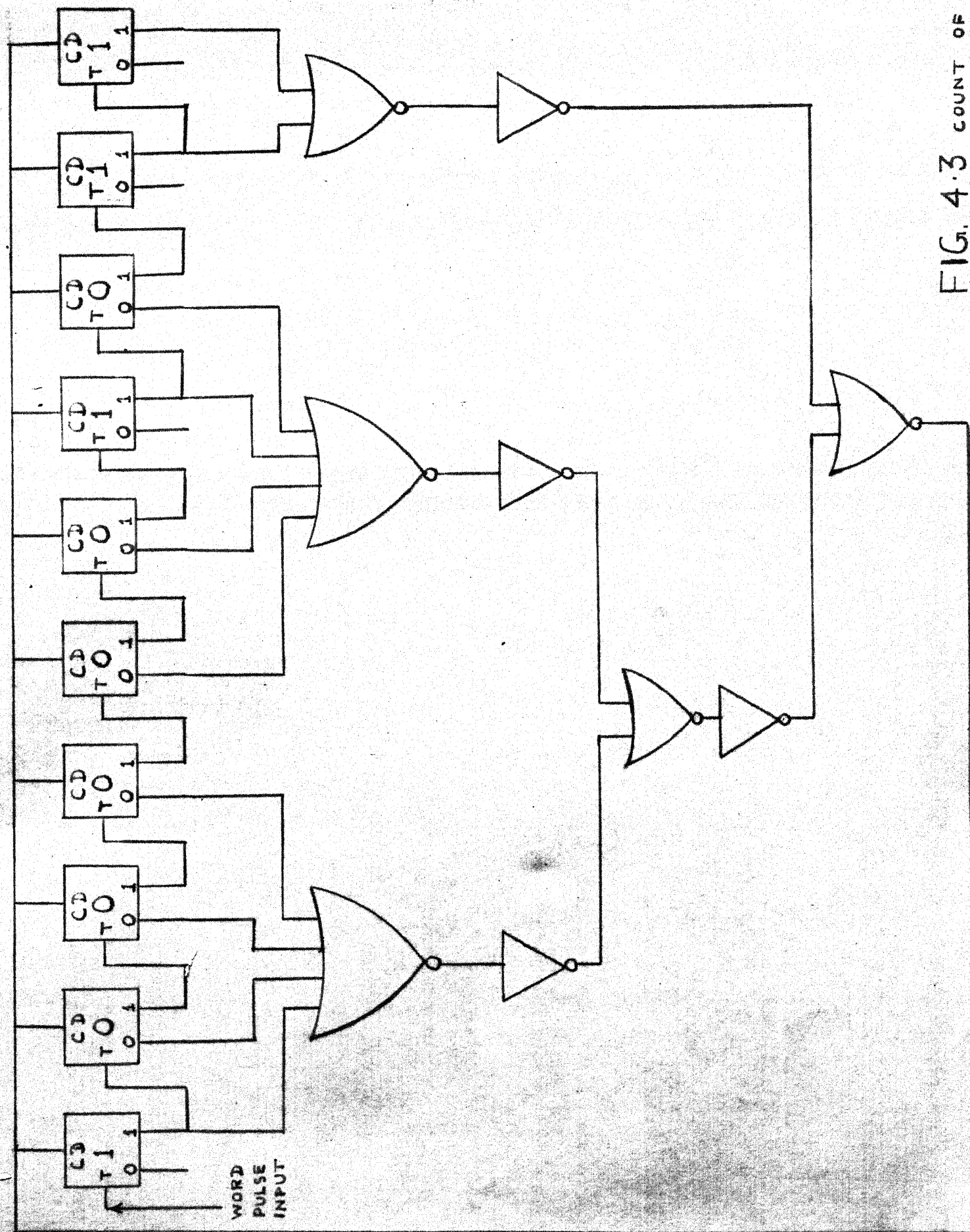
4 3 Counter

As pointed out earlier, the setting of the counter
is freely adjustable according to the requirements of any
particular application. In the present setup, we have
connected the flip-flops to count upto 500 words, as shown
in Fig.4.3. The outputs 1, 0, 0, 0, 0, 0, 1, 0, 1, 1 from
flip-flops 1 through 10 are fed to a ten-input AND gate
which is identical to the one used in the coincidence unit
(Fig.4.2). The AND gate produces an output pulse at the end
of 500 count to clear all the flip-flops.

The flip-flops used are Motorola dual JK flip-flop
(MC 890-P).

.4 Decoder

Depending upon the track number in the Address
Register one of the channel will be energised. The ten
different channels have been given ten different codes. As
an example, to select channel one, which has been assigned
the channel selecting bits 0011 (say), the output, 0,0,1
and 1 from the Address Register are fed to a AND gate to get
a pulse output. This output pulse opens another six-diode
gate and permits the signal to enter or leave the drum on
the selected channel.

The channel selection address register consists of
four flip-flops (MC 890-P) with fanout of three only. To

otain a uniform fanout from each flip-flop five pairs of
complementary numbers, as shown below, have been choosen
for the ten channels.

0	0	1	1	Channel-1
0	1	0	0	Channel-2
0	1	0	1	Channel-3
0	1	1	0	Channel-4
0	1	1	1	Channel-5
1	1	0	0	Channel-6
1	0	1	1	Channel-7
1	0	1	0	Channel-8
1	0	0	1	Channel-9
1	0	0	0	Channel-10

The above channel selecting bits demand a fanout of five
from each flip-flop. This is achieved by connecting the
output of each flip-flop to a buffer (MC 889-P). Each
buffer (MC 889-P) has a fanout of five. The complete logic
circuit is shown in Fig.4.4.

4 5 <u>Gate</u>

The Fig.4.5 shows the arrangement of a six diode gate.
One such gate has been used in each channel.

When the control voltages are V_n and $-V_n$, diodes D_5
and D_6 get forward biased and diodes D_1, D_2, D_3, D_4 get
reverse-biased, so that the gate is closed. On the other hand
when the control voltages are V_c and $-V_c$, diodes D_5 and D_6 get
reversed-biased and make diodes D_1 through D_4 to conduct,
resulting in the transmission of signal through the gate.
V and $-V$ are the fixed voltages.

The control voltages are obtained from the flip-flop.
The duration for which the gate remains open is controlled by
a one-shot multivibrator. One quad two-input NOR gate
(MC 824-P) is used for this purpose (Fig.4.6). The resistance
R and the capacitance C are the timing elements. The opera-
tion of the circuit can be explained as follows.

Under steady state condition the points 'a' and 'b' are
at high level, corresponding to '1', the point 'd' is at low
level, corresponding to '0'. On application of a trigger at
the trigger terminal 12, the point 'b' is brought down to low
level. The sudden change in potential at the point 'b' is also
communicated to the point 'a' through the capacitor C. The
potential at 'a' then rises with time constant $= 0.33$ RC
till it reaches the cut-in voltage V_r. When the cut-in

−6V

4·7K   68pf   68pf   4·7K

30K   30K

2N995   2N995

10k   510 Ω   10k

+6V

0·1µf

820 Ω

2N995   68pf

47k   i/p

75k

D5   CD21   D3   CD21   D4   CD21   CD21   D6

−Vn or +Vc   +Vn or −Vc

(V)   CD21   CD21   (−V)
+3V   10K   D1   D2   10K   −3V

FIG 4·5 SIX DIODE GATE

+Vcc

R

b   c   a   1
          2   3   d   13
                              12   14   7   5   1

TRIGGER INPUT   6

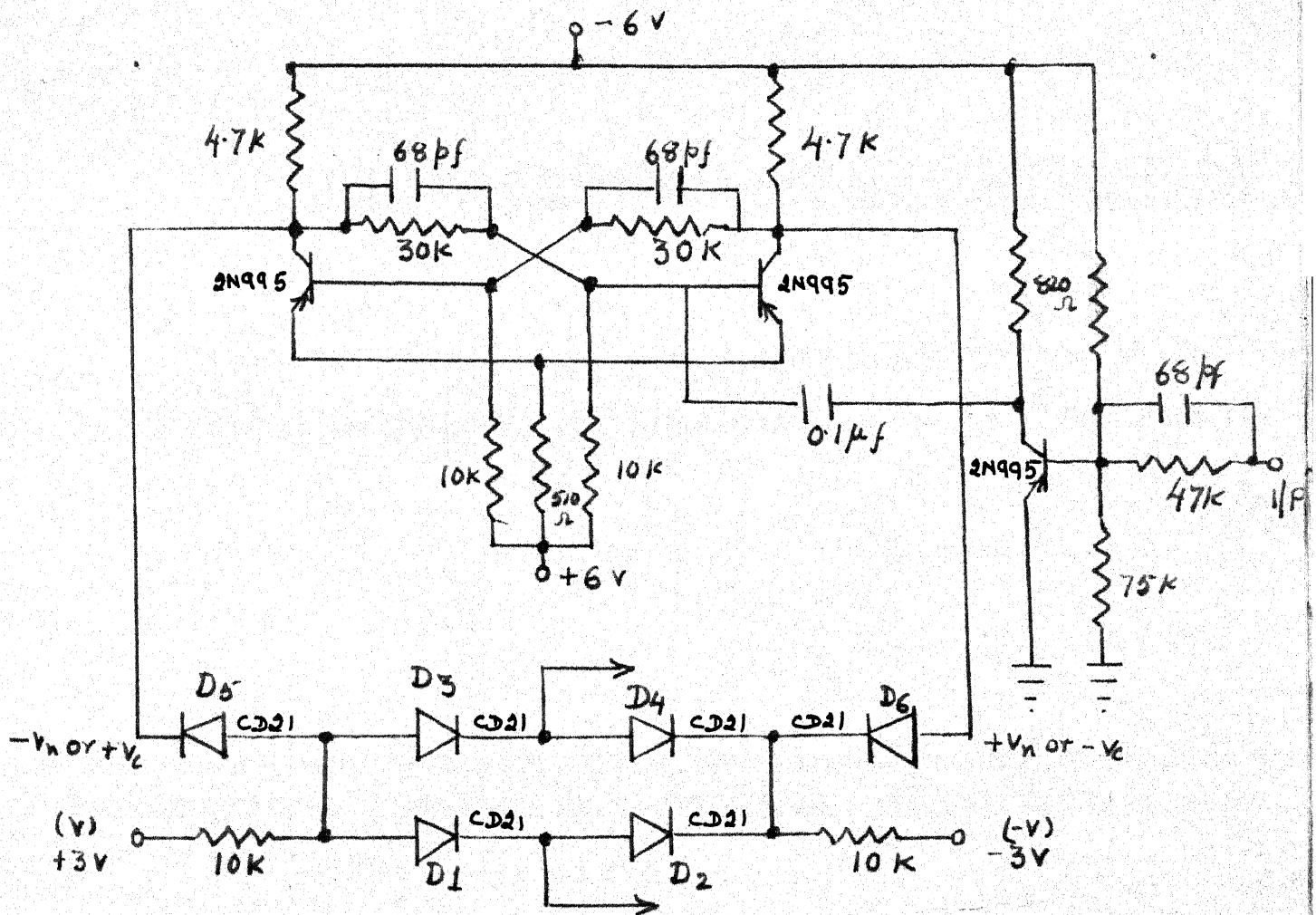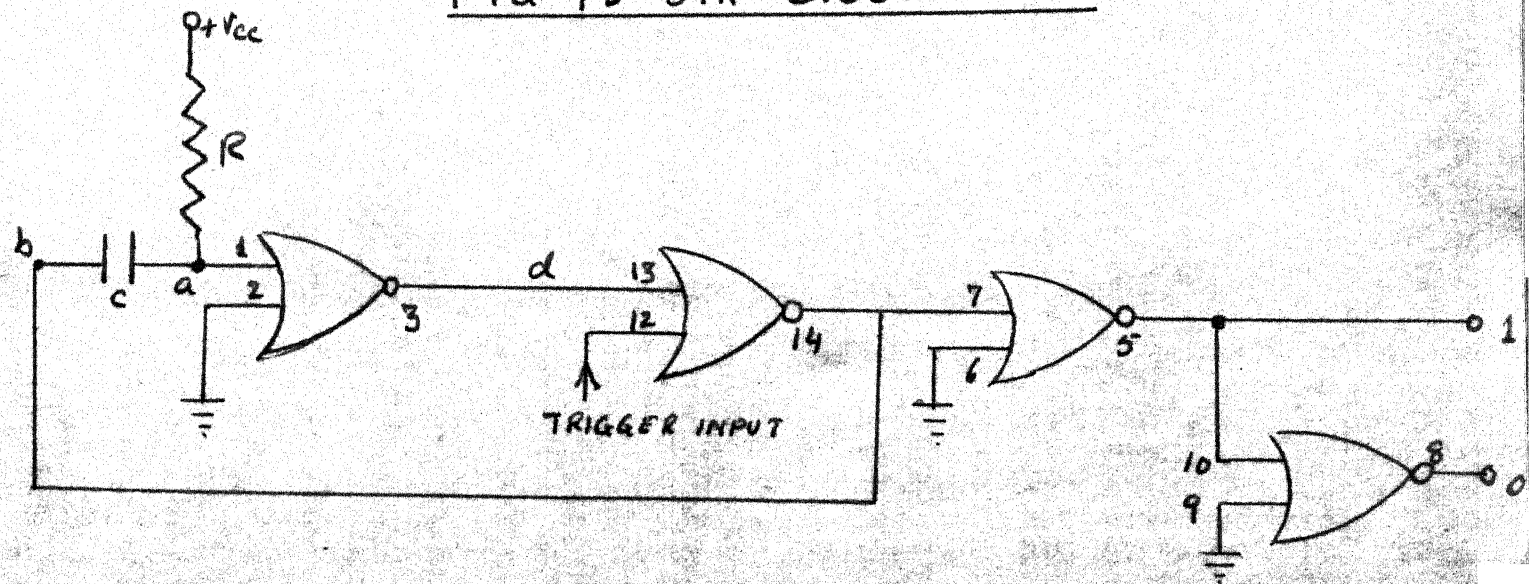10   8
9   0

FIG 4·6   MONOSTABLE MULTIVBRETOR.
(USING MC824P)

volt e is reached the potential at'd'comes down to zero
nd this inturn makes the points'a'and'b'of equal potential.
The two complementary outputs from the monostable can be
obtained from the terminals 5 and 8.

4.6 Write Amplifier

The requirements for the write amplifier are as
follows.

(a) The write current should be of the order of
200 milliamps.

(b) Output impedance at 140 KHz = 100 ohms.

(c) The positive information pulse, corresponding to '1',
should only be able to change the state from higher
saturation level to lower saturation level.

(d) The negative information pulse, corresponding to '0'
should only be able to change the state from lower
saturation level to the higher saturation level.

(e) The clock pulses, chosen to be negative, should be
able to change the state irrespective of the existing
saturation level. In other words if the previous
state is at higher saturation level the clock pulse
will change the state to lower saturation level and
vice-versa.

Keeping the above requirements in view the write
amplifier is designed by making use of a flip-flop using

p-n-p transistors T_3 and T_4 (Fig. 4.8). The negative clock pulses are applied at the base of the inverters T_2 and T_5 through the diodes D_1 and D_2 and hence the flip-flop is switched whenever clock pulse comes. The positive information pulses are first inverted by T_1 and then fed at the base of inverter T_2 to trigger the flip-flop, whereas the negative pulses are directly applied at the base of the inverter T_5 through the diode D_4. Thus a positive information pulse makes the output voltage Y low if Y is originally high, while the state is unchanged if Y is originally low. The effect of a negative information pulse is just the other way round. The outputs Y and $\overline{Y}$ are applied to a push-pull emitter-follower pair using transistors T_6 and T_7 or T_8 and T_9 respectively. The emitter-follower pairs are used to supply the bi-directional current drive needed by the heads. Thus we obtain the write current waveform corresponding to any given sequence of information pulses as required by the scheme elaborated in Section 3.4.

4.7 Read Amplifier

The magnetic drum read amplifier for phase recording (Fig. 4.7) consists of three stages. The first stage is a common-base stage consisting of transistor T_1 which provides a low input impedance to the head winding. The bias voltage of +1 volt in the emitter circuit generated by means of a
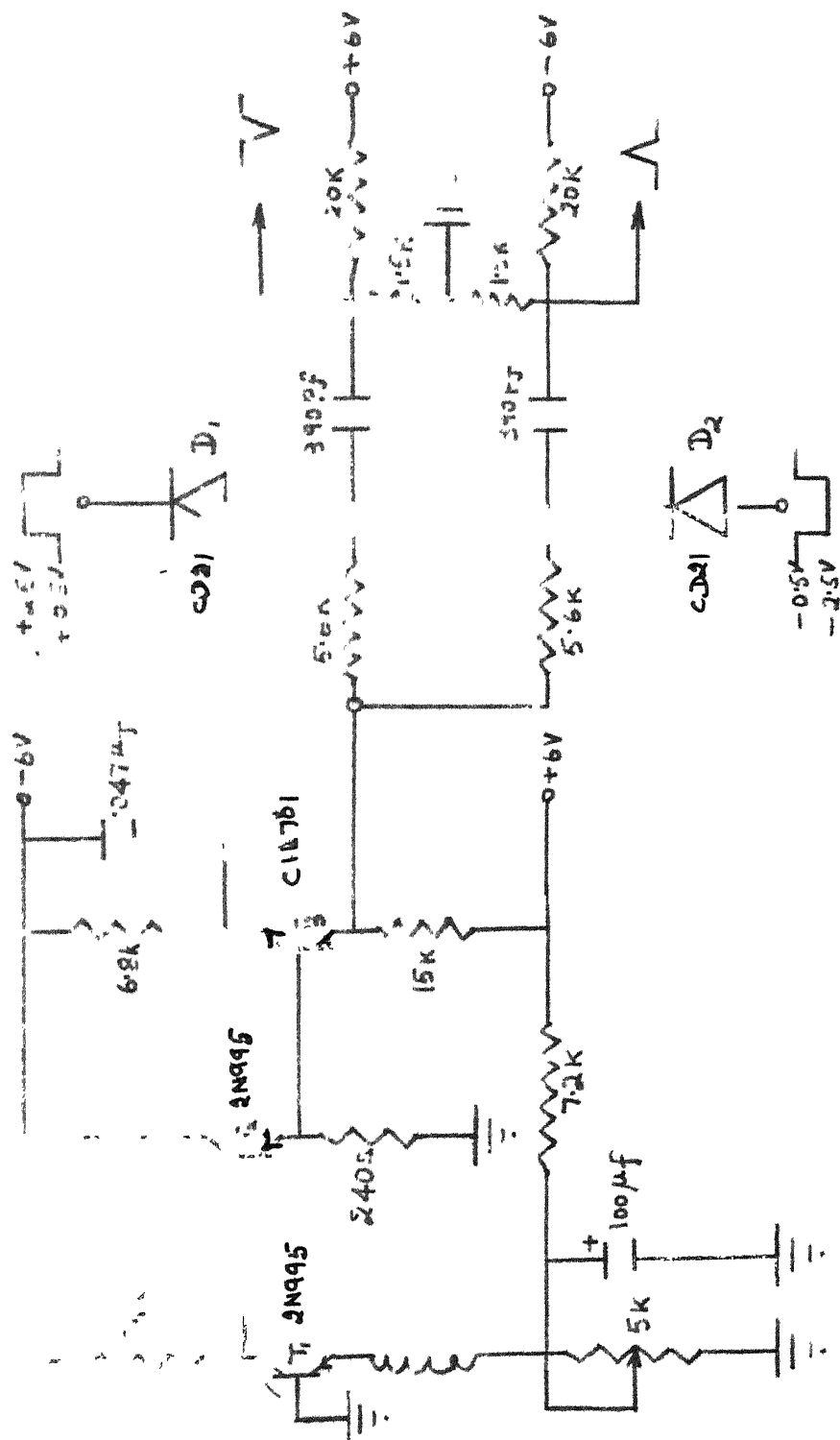
FIG. 4.9 READ AMPLIFIER

rual tive potential divider and a bypass capacitor C, serves
to accomplish an adequate initial current level so that
amplification of the signal occurs in the linear portion of
the transistor characteristic.

The second stage consisting of transistor T_2,
constitutes an emitter-follower which acts as an impedance
matching stage between common-base stage and the common-
emitter stage, which provides the final amplification. The
output voltage is symmetrical with respect to ground, i.e.,
in the absence of signals the collector voltage of T_3 is
close to zero, while opposite polarities of the signal read
by the head winding cause output voltages of opposite
polities.

The output from T_3 is then strobed so that the
output voltage is transmitted only if a clock pulse is
present. The strobing circuitry consists of shunt clippers
using diodes D_1 and D_2 which are reverse-biased when a clock
pulse is present, and forward biased in absence of a clock
pulse. By adjusting the height of the clock pulse, one can
decide the final output voltage level. The RC circuit
following the diodes constitute differentiators which gives
the final output voltages in the form of trigger.

4.6 Schematic Diagram

The detailed schematic of the READ/WRITE System is shown in the foldout at the end of the report.

REFERENCES

1.   Hoagland, A.S., Magnetic drum recording of digital
        data, Trans. AIEE, Vol.73, Pt.I, September, 1954,
        pp. 381-385.

2.   Booth, A.D., A magnetic drum digital storage system,
        Electronic Engineering, Vol.21, July, 1949, pp.234-238.

3.   Bivans, E.A., Synchronizing magnetic drum storage
        speed, Electronics, Vol.28, No.8, August, 1955,
        pp. 140-141.

4.   Williams, F.C., and West, J.C., Position synchronization
        of a rotating drum, Proceedings of the Institute of
        Electrical Engineers, Vol.98, Pt.II, February, 1951,
        pp. 29-34.

5.   Parry, I.W., and Maudsley, B.G., Proceedings of the
        Institute of Electrical Engineers, Vol. 103, Part B,
        Suppliment No.2, April, 1956, pp. 197-202.

6   Richards, R.K., Digital computer components and
        circuits, D. Van Nostrand Co., Princeton, N.J., 1957.

7.   Ware, H.W., Digital computer technology and design,
        Vol.II, The RAND Corporation, Santa Monica, California.

8.   Smith, C.V.L., Electronic digital computers, McGraw-Hill
        Book Co., New York, 1959.

9. Wallace, R.L. Jr., The reproduction of magnetically recorded signals, Bell System Technical Journal, Vol.30, October, 1951, pp. 1145-1173.

10. Fuller, H.W. et al., Techniques for increasing storage density of magnetic drum systems, Proceedings of the 1954 Eastern Joint Computer Conference, Philadelphia, 8-10 December, 1954, pp. 16-21.

11. Millman, J. and Taub, H., Pulse, Digital and Switching waveforms, McGraw-Hill Book Co., New York, 1965.

12. Pressman, A.I., Design of transistorized circuits for digital computers, John F. Rider Publisher, New York, 1959.

13. Mazumdar, S., One megacycle universal logic module, Master's Thesis EE-15-1968, Department of Electrical Engineering, Indian Institute of Technology, Kanpur, August, 1968.